IN THE SPECIFICATION:

Kindly replace the paragraph beginning on page 2, line 10, with the following:

The present invention is related to the following commonly-assigned, copending applications:

"Multi-Mode Iterative Detector", filed on April 27, 2000 and assigned application Serial No. 09/559186, the contents of which are incorporated herein by reference,

"Address Generator for LDPC Encoder and Decoder and Method Thereof", filed on even date and assigned application Serial No. 09/730,597 (Attorney Docket No. MP0063), the contents of which are incorporated herein by reference,

"LDPC Decoder and Method Thereof", filed on even date and assigned application Serial No. 09/730,603 (Attorney Docket No. MP0065), the contents of which are incorporated herein by reference, and

"Parity Check Matrix and Method of Forming Thereof", filed on even date and assigned application Serial No. 09/730,598 (Attorney Docket No. MP0069), the contents of which are incorporated herein by reference.

Kindly replace the paragraph beginning on page 3, line 5, with the following:

The operation of transmission section 300 will now be explained. Prior to processing by transmitting section 300, input or user data maybe encoded with an error correcting code, such as the Reed/Solomon code, or run length limited encoded (RLL) or a combination thereof by encoder 302. The encoded output encoder 302 is then interleaved by deinterleaver 308 for input to linear block code encoder 304 which generates parity data in a known manner utilizing linear block codes. One example of a linear block code is a low-density parity-check code (LDPC) which is discussed by Robert G. Gallager in *Low-Density Parity-Check Codes*, 1963, M.I.T. Press and by Zining Wu in *Coding and Iterative Detection For Magnetic Recording Channels*, 2000, Kluwer Academic Publishers, the contents of each of

which are incorporated in their entirety by reference. Deinterleaver 308 permutes the data so that the same data is reordered before encoding by linear block code encoder 304. By permuting or redistributing the data, ~~interleaver~~ deinterleaver ~~306~~ 308 attempts to reduce the number of nearest neighbors of small distance error events. User data at the output of encoder 302 is referred to as being in the channel domain; that is the order in which data is transmitted through the channel. The order of data processed by deinterleaver 308 is referred to as being in the linear block code domain. The parity data from linear block code encoder 304 is combined with the data encoded by encoder 302 by multiplexer 306 for input to channel transmitter 310.

Kindly replace the paragraph beginning on page 3, line 24, with the following:

Transmitter 310 transmits the combined user and parity data from multiplexer 306 typically as an analog signal over communication channel 401 in the channel domain. Communication channel 401 may include any wireless, wire, optical and the like communication medium. Receiver 500 comprises a front-end circuit 502 comprising analog to digital and equalization circuits. The digital signal front-end circuit 502 is input to soft channel decoder 504, which provides probability information of the detected data. Soft channel decoder 504 may be implemented by a Soft Viterbi Detector or the like. The output of the soft channel decoder 504, which is in the channel domain, is converted into the linear block code domain by deinterleaver 510. Deinterleaver 510 is constructed similarly to deinterleaver 308. Soft linear block code decoder 506 utilizes this information and the parity bits to decode the received data. One output of soft linear block code decoder 506 is fed back to soft channel decoder 504 via interleaver 512, which converts data in the linear block code domain to the channel domain. Interleaver 512 is constructed to perform the reverse operations of deinterleaver 510. Soft channel decoder 504 and soft linear block code decoder 506 operate in an iterative manner to decode the detected data.

Kindly replace the paragraph beginning on page 4, line 12, with the following:

Fig. 2 is a block diagram of a data transmission system implementing an address generator in lieu of the interleave/deinterleaver. A more detailed description of this system can be found in commonly assigned copending application "Address Generator for LDPC Encoder and Decoder and Method Thereof" filed on even date and assigned application Serial No. 09/730,597 (Attorney Docket No. MP0063), the contents of which are incorporated herein by reference. In general as shown therein, a digital data transmission system comprises a transmitting section 300' for transmitting user data to receiver 500' via communication channel 401. The inventors have observed that a linear block code encoder is not dependent on a position of a bit interleaved. Rather the linear block code encoder only requires a list of equations for a given bit. In other words, there is no need to process the data in the order defined by the interleaver, instead data may be processed in the same order as it is written to the channel. This can be accomplished by incorporating an address generator to provide an address of the appropriate equation of the linear block code encoder. This principle can be similarly applied to the soft linear block decoder. As a result, deinterleaver 308 of the conventional system is now replaced by address generator 328, and deinterleaver 510 is now replaced by address generator 530. Accordingly, there is no requirement for the physical interleaving of data in the receiver 500', since the data remains in the same order as the order of bits of data in the channel throughout this system. The order of bits of data transmitted through the channel is referred to as the channel domain.

Kindly replace the paragraph beginning on page 10, line 4, with the following:

Soft linear block code decoder 506 operates in combination with soft channel decoder 504 and address generator 530 in an iterative fashion. Soft linear block code decoder is preferably implemented as a low-density parity- check code (LDPC) decoder as described in commonly assigned, copending patent application entitled "LDPC Decoder and Method Thereof", filed on even date and assigned application Serial No. 09/730,603 (Attorney Docket No. MP0065), the contents of which are incorporated herein by reference.

Kindly replace the paragraph beginning on page 12, line 9, with the following:

The process of calculating u is as follows. As data is provided from encoder 302 to linear block encoder 304, the process begins to calculate the parity data. In other words, it is not necessary to have the entire codeword to begin calculating the parity data. As the data is provided from encoder 302 to linear block code encoder 304, address generator 328 provides row information indicating the equation utilized b the user data. Commonly assigned, copending application entitled "Address Generator for LDPC Encoder and Decoder and Method Thereof" filed on even date and assigned application Serial No. 09/730,597 (Attorney Docket No. MP0063), the contents of which are incorporated herein by reference, provides a detailed description of address generator 328.